ABSTRACT OF THE DISCLOSURE

A fault analysis method and apparatus which is able to improve the reliability of fault analysis of semiconductor integrated circuit. In case of supplying a test pattern sequence having a plurality of test patterns to the semiconductor IC, an analysis point whose electric potential changes according to the change of supplied test pattern is placed corresponding to the test pattern sequence. Then, a transient power supply current generated on the semiconductor IC according to the change of the test pattern is measured and determined whether the measured transient power supply current is abnormal or not. A defection point is presumed based on the test pattern sequence where the transient power supply current is abnormal, and the analysis point placed corresponding to the test pattern sequence.